What is claimed is:

1. A semiconductor memory device capable of minimizing a data accessing time, comprising:

a first control signal generating means for outputting a first control signal generated by logically combining a pipelatch-in signal and a start-odd start-even data output control signal;

a second control signal generating means for outputting an odd control signal generated by logically combining an odd data enable signal for outputting odd-numbered data and a control signal for accessing the odd-numbered data in response to a start address, and outputting an even control signal produced by logically combining an even data enable signal for outputting even-numbered data and a control signal for accessing the even-numbered data in response to the start address;

a first data accessing means for accessing inputted data under the control of the first control signal outputted from the first control signal generating means;

a latching means for temporarily storing data outputted from the first data accessing means; and

a second data accessing means for secondly accessing the data stored at the latching means and outputting secondly accessed data.

2. The semiconductor memory device of claim 1, wherein

the first control signal generating means includes:

an inverter receiving the pipelatch-in signal;

a first NAND gate receiving an output of the inverter and the start-odd start-even data output control signal to thereby output a piseso signal; and

a second NAND gate receiving the output of the inverter and an output of the first NAND gate to thereby output a pisose signal.

3. The semiconductor memory device of claim 2, wherein the second control signal generating means includes:

an odd data accessing control signal producing means for outputting the odd control signal generated by logically combining the odd data enable signal for outputting the odd-numbered data and the control signal for accessing the odd-numbered data in response to the start address; and

an even data accessing control signal producing means for outputting the even control signal created by logically combining the even data enable signal for outputting the even-numbered data and the control signal for accessing the even-numbered data in response to the start address.

4. The semiconductor memory device of claim 3, wherein the odd data accessing control signal producing means has:

a first inverter receiving the odd data enable signal for outputting the odd-numbered data;

a first NAND gate receiving an output of the first

inverter and the control signal for accessing the odd-numbered data in response to the start address;

a second NAND gate receiving the output of the first inverter and an output of the first NAND gate;

a second inverter for inverting an output of the second NAND gate;

a third inverter for inverting the output of the first NAND gate;

a third NAND gate receiving an output of the second inverter and a rising edge synchronization signal outputted synchronized with a rising edge of a clock pulse to thereby output a pre-odd data output control signal; and

a fourth NAND gate receiving the rising edge synchronization signal and an output of the third inverter to thereby output a post-odd data output control signal.

5. The semiconductor memory device of claim 3, wherein the even data accessing control signal producing means has:

a first inverter receiving the even data enable signal for outputting the even-numbered data;

a first NAND gate receiving an output of the first inverter and the control signal for accessing the even-numbered data in response to the start address;

a second NAND gate receiving the output of the first inverter and an output of the first NAND gate;

a second inverter for inverting an output of the second NAND gate;

a third inverter for inverting the output of the first NAND gate;

a third NAND gate receiving an output of the second inverter and a falling edge synchronization signal outputted synchronized with a falling edge of a clock pulse to thereby output a pre-even data output control signal; and

a fourth NAND gate receiving the falling edge synchronization signal and an output of the third inverter to thereby output a post-even data output control signal.

6. The semiconductor memory device of claim 5, wherein the first data accessing means includes:

a first transmission gate for outputting data on a first multiplexer even data output line under the control of the pisose signal;

a second transmission gate for outputting data on a first multiplexer odd data output line under the control of the piseso signal;

a third transmission gate for outputting data on a second multiplexer even data output line under the control of the pisose signal; and

a fourth transmission gate for outputting data on a second multiplexer odd data output line under the control of the piseso signal,

wherein output nodes of the first and the second transmission gates are connected to each other and output nodes of the third and the fourth transmission gates are attached to each

other.

7. The semiconductor memory device of claim 6, wherein the latching means includes:

a first plurality of inverters connected with the output node of the first transmission gate inversely and in parallel; and

a second plurality of inverters connected with the output node of the third transmission gate inversely and in parallel.

8. The semiconductor memory device of claim 7, wherein the second data accessing means outputs data provided from the first plurality of inverters under the control of the pre-odd data output control signal and outputs data fed from the second plurality of inverters under the control of the post-odd data output control signal.